A MULTI-CHANNEL LOW-POWER CIRCUIT FOR IMPLANTABLE AUDITORY NEURAL RECORDING MICROSYSTEMS

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Abstract: A multi-channel low-power circuit for auditory neural signal processing from multi-channel microprobes for implanting in the auditory nerve has been designed and simulated. The chip is being fabricated with the AMI 0.5 µm triple-metal double-poly CMOS process with a die size of 1.5 × 1.5 mm. Low-noise and low-power preamplifiers are designed to pick up the weak signals from each microelectrode with a gain of 36 dB, bandwidth from 5 Hz to 7.2 kHz, and a power consumption of 98 µW. Analog time division multiplexers (MUX) are used for each group of eight electrodes to conserve external leads and discriminate signals from different recording sites with a power dissipation of 0.04 µW per multiplexer. An 8-bit successive approximation Analog-to-Digital Converter (ADC) is designed to digitize the analog signals. The ADC consumes 0.84 µW at 1.5 V supply with a sampling rate 100 kS/s. The overall power dissipation per channel is less than 100 µW.

Introduction

Over the past several decades, researchers have attempted to restore hearing function by replacing damaged auditory pathways with electrical circuits. Auditory prostheses for profoundly deaf patients are feasible because auditory perception can be successfully activated by electrical stimulation of the nervous system via electrode implanted into the cochlea [1]. Direct stimulation of auditory nerve would offer significant advantages over cochlear implant by providing increased spectral resolution and low power consumption. However, the tonotopic map of the human auditory nerve has not been definitively identified. The recording of multi-channel neural electrical activity with microelectrode array is desirable for determining the frequency map for human auditory nerves.

We have previously reported a silicon three-dimensional, high density passive microelectrode array for auditory nerve implant [2, 3]. A 100-channel electrode array was created in a 1 mm^2 area with a combination of deep reactive-ion etching (DRIE) and hydrofluoric-nitric-acetic acid (HNA) wet etch bulk micromachining technology (Fig. 1).

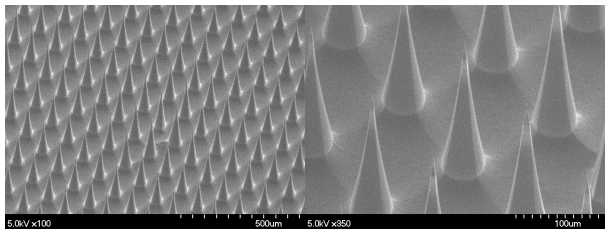

Figure 1: Scanning electron micrographs (SEM) of the micromachined electrode array for auditory neural implant.

Due to the weak electrical signals detectable from nerve fibers and typical high impedance of the implant electrodes, there is a great demand to integrate signal processing circuits with the microelectrode arrays. Furthermore, long electrical interconnects between the implanted probes and signal processing circuits can be eliminated, drastically improving device packaging, device signal-to-noise ratio, mechanical reliability, and ease of surgical procedure.

In this paper, we present the design, simulation and layout of a multi-channel low-power circuit for auditory neural signal recording and processing, which will be integrated with the micro-fabricated neural probe array with flip-chip bump-bonding technology (Fig. 2). We show that the overall power consumption per channel is less than 100 µW.

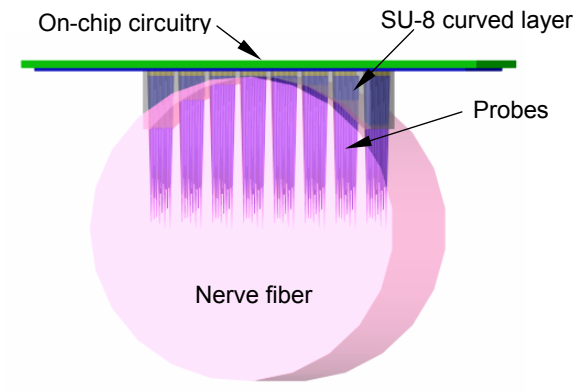

Figure 2: Conceptual drawing of the microelectrode array integrated with on-chip circuitry.

System Design

1. Design Requirements

For chronic neural signal recording and processing, the implantable device must be designed with a strict system power budget compatible with the power delivery approach. In addition, the need to avoid potential thermal damage of surrounding tissues due to excessive heat dissipation from the implanted device places additional constraints on the circuits. A heat flux of 80mW/cm^2 has been reported to cause necrosis in muscle tissue [4]. In our current design, the chip size is 2.25 mm^2, so the power dissipation should less than 1.8 mW.

Increasing demand for larger numbers of electrodes and higher spatial recording resolution from multi-channel recording constitute important functional design requirement. In cochlear implants, 8 to 16 channels are routinely required to restore functional speech perception in profoundly deaf patients. However, to restore music appreciation, for example, potentially far more frequency channels and frequency resolution are required. We have created and reported on the design and fabrication of a 100-channel microelectrode array in prior work [2, 3] for use in studying the tonotopic characteristics of the auditory nerve.

Typical measured signal magnitudes of neuronal action potentials range between 50 and 500 μV, depending on the measurement setup. In some cases, the impedance of a single channel silicon electrode can be as high as 100 MΩ, resulting in very weak signal-to-noise ratio. In addition to lowering the probe impedance by coating with gold, for example, low-noise signal amplification is necessary for downstream signal processing, which includes multiplexing and analog-to-digital conversion. Finally, it should be noted that neural signal energy spectrum typically spans from 100 Hz to 7 kHz range [5], where an average MOSFET device shows an undesirably high level of noise spectral density [6], representing a unique constraint in the design of low-noise amplifiers.

2. System Architecture

Figure 3 shows a block diagram of a 64-channel neural signal recording circuit. Because of the need to amplify weak neuronal signals in a noisy environment, one low-noise pre-amplifier is dedicated to each active microelectrode. A time-division multiplexer is employed for each group of eight electrodes to reduce the number of external leads and to discriminate signals from different recording sites. The multiplexed signals are then amplified with a second-stage operational amplifier, which is then digitized with an 8-bit A/D converter.

This system architecture can be scaled to 96 channels or more by further reducing the power requirement per channel.

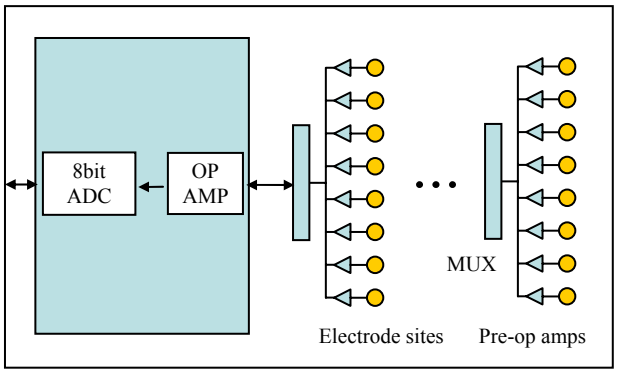

Figure 3: Block diagram of a 64-channel on-chip neural signal recording circuit.

3. Low-noise pre-amplifier

Figure 4 is the schematic of the closed-loop pre-amplifier design. The close loop gain is set by the capacitance ratio C_1/C_2, where C_1 (and the load capacitor C_L) are much larger than C_2.

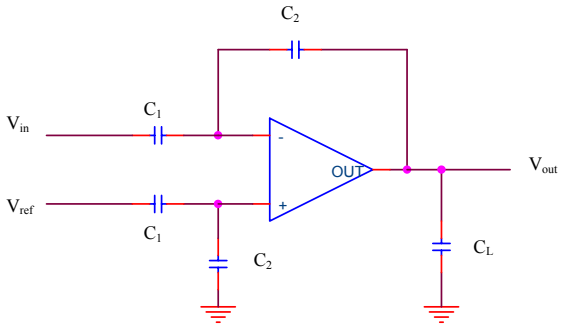

Figure 4: Schematic of the closed-loop neural recording pre-amplifier.

Within the frequency range of the neuronal signals, the main noise source within the system is flicker noise, or $1/f$ noise, from the MOSFET devices. Its noise spectral density, $N_{1/f}(f)$, can be express as

$$N_{1/f}(f) = \frac{K}{C_{ox}WL}\frac{1}{f^{\alpha}} \qquad (1)$$

where L and W are the gate length and width of the transistor, respectively; C_{ox} is the gate-oxide capacitance per unit area; K and α are parameters that are related to specific fabrication processes [7]. The equation shows that the noise spectral density is inversely proportional to the gate area of the transistors. Therefore, a large gate area at the input transistor of the amplifier is necessary to reduce $1/f$ noise. However, a conflicting requirement for multi-channel recording is the need to minimize the area of the design in order to implement one dedicated amplifier for each recoding electrode. Thus, we need to minimize the areas of amplifiers at the input stages while meeting the specification for the noise requirement for the following system [8].

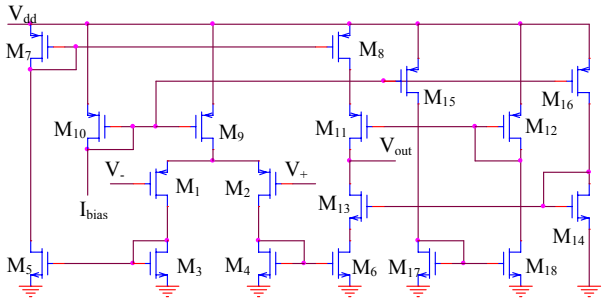

Figure 5: Circuit diagram of the operational transconductance amplifier used in the pre-amplifier.

Figure 5 shows the design of the operational transconductance amplifier (OTA) used in the neural recording pre-amplifier. Two identical PMOS transistors (M_1 and M_2) with larger gate areas, and thus lower $1/f$ noise than those in NMOS transistors [8], are used at the input stage. Transistors M_3–M_6 are designed to be a matched pair, and so are transistors M_7–M_8. Transistors M_9–M_{18} generate the bias current and voltages for the circuit. The voltage supply is 3V, with a bias current set at 8 µA, giving devices M_1 – M_8 drain currents of 4 µA each. At this current level, each transistor may operate in weak, moderate, or strong inversion depending on it W/L ratio [9]. The simulation result (Fig. 6) illustrates that the closed-loop gain for the current design is about 36 dB. The total DC power consumption is 98 µW.

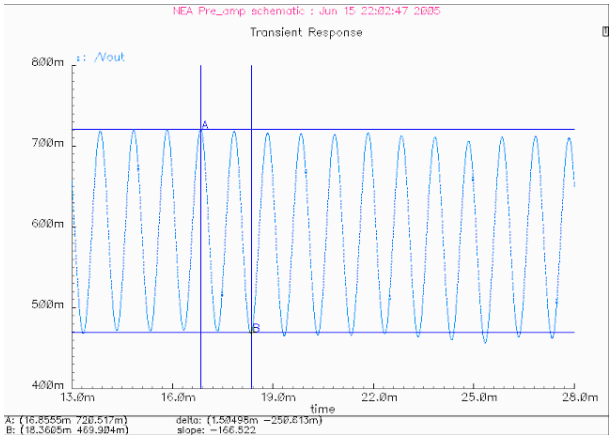

Figure 6: Simulation result of the closed-loop gain of the preamplifier.

4. 8-bit ADC

The charge-redistribution successive-approximation A/D converter is chosen in this design for the minimal amount of analog circuitry required, which satisfy our primary design goal of low power consumption and small layout area [7]. The successive conversion approach uses a binary search algorithm to determine the closest digital word to match an input signal.

As shown in Fig. 7, the successive approximation architecture, which is similar to the design reported in [10], employs a comparator, a successive approximation register (SAR) and a switch network to implement the search algorithm.

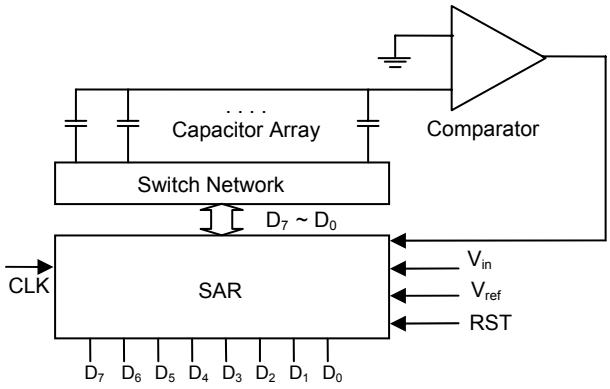

Figure 7: Architecture of successive approximation ADC.

The operation of the ADC is as follows. In the first step, all the capacitors are charged to the input voltage. Then, all the capacitors are switched to ground and the SAR generates an approximation. The sum of the input voltage and the approximation is compared to the reference voltage, which is zero in our case, by the comparator. The SAR uses the comparator result to generate its next approximation for the digital code. The process is repeated N times, with a smaller capacitor being switched each time, until the conversion is finished.

The ADC is powered with 1.5V at 300 nA bias current. The power consumption is 0.84 µW. The sampling rate is 100 KS/s. The resolution of the ADC is 8 bit. And the unit capacitance of the capacitor array is 12 fF.

5. Analog MUX

A full CMOS switch 8:1 multiplexer (MUX) is developed in this work. One MUX has eight data inputs (D_0 ~ D_7), three address inputs (A_0 ~ A_2) and one data output. Figure 8 shows the circuit of the full CMOS switch used in the MUX. The power dissipation for the MUX is 0.04 µW.

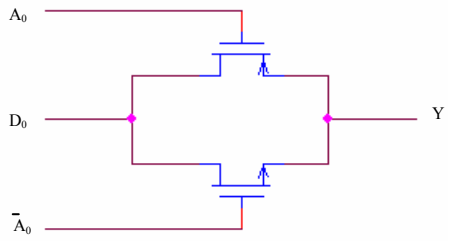

Figure 8: The full CMOS switch for the multiplexer.

Circuit Layout

The multi-channel neural recording chip is fabricated with the AMI 0.5 µm triple-metal double-poly CMOS technology with a die size of 1.5 mm × 1.5 mm (Fig. 9). The layouts for all circuit blocks are quite conservative to ensure that crosstalk and parasitic capacitance are minimized. In the block with capacitors, the most area is taken by the capacitors. The die area could be reduced for future design with a denser capacitor array.

The layout area of ADC, as shown in Fig. 9, occupies 0.127 mm^2. As noted in [11], the matching and noise in the capacitor array determines the accuracy of the A/D converter. Poly-poly capacitors are used with the top plates acting as the common plate. This minimizes parasitic capacitance at the comparator input [10]. The layout for the capacitor array employs a common-centroid structure and dummy capacitors on the edges of the array. Table 1 summarizes the performance of each circuit component and the overall design.

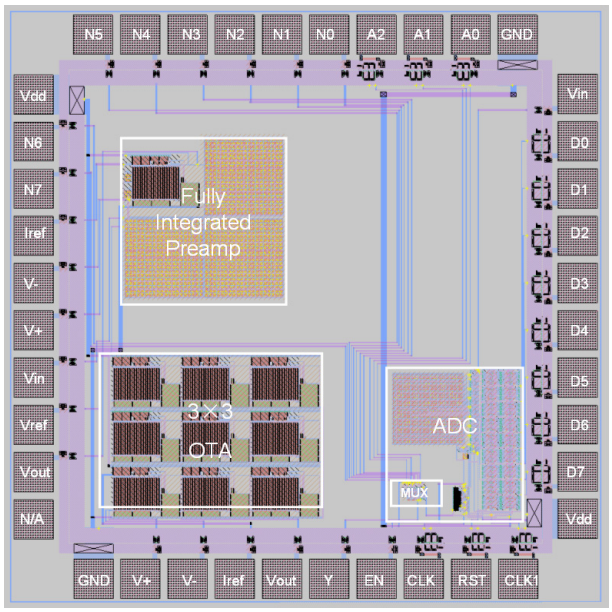

Figure 9: Overall layout of the neural recording chip.

Table 1: Neural recording chip performance summary.

Circuit Blocks	Specification	Power Consumption
Pre-amplifier	Supply voltage: 3 V Gain: 36 dB Bandwidth: 7.2 KHz Noise: 9 µVrms	98 µW
ADC	Supply voltage: 1.5 V Speed: 100 KS/s Resolution: 8 bit	0.84 µW
MUX	8:1	0.04 µW
Overall	Die size: 2.25 mm^2 AMI 0.5 process	98.88 µW

Conclusions

A multi-channel low power auditory neural signal recording circuit has been reported. It includes low-noise pre-amplifiers, analog multiplexer and A/D converter. The circuit bump-bonded to the microelectrode array will be implanted onto the auditory nerve to characterize the tonotopicity. We achieve a total power consumption <100 µW. Results of on-going chip characterization will be reported in the near future.

Acknowledgement

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